

PATENT ABSTRACTS OF JAPAN

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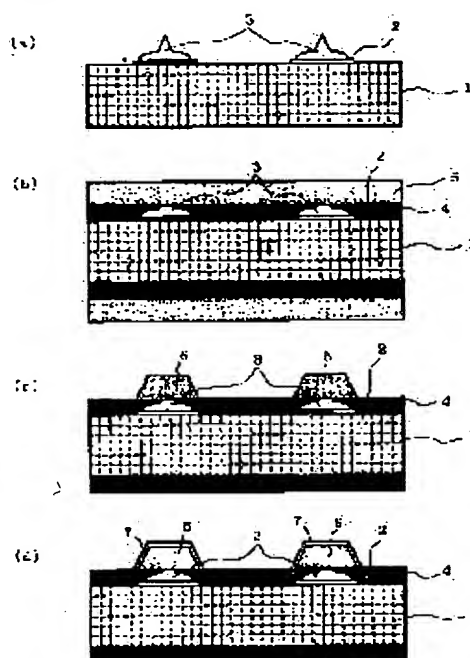
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(54) TERMINAL FORMING METHOD FOR WAFER LEVEL CSP

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for forming a terminal of a wafer level CSP by using a pointed gold bump formed by a wire bonding method as it is without leveling and further forming a package electrode directly on the bump.

SOLUTION: A sharp gold bump is formed on an aluminum electrode or copper electrode on the top surface of a semiconductor wafer by a conventional method using a wire bonder, and copper foil with resin is laminated by being heated and pressed. Here, the copper foil thickness is about 75 μm and the resin thickness is 50 to 60 μm depending upon the size of the bump, the sharp tip of the gold bump is pressed and crushed by the copper foil, and the gold bump and copper foil are fixed with epoxy resin while electrically connected by press contacting. Then an electrode is formed by etching the copper foil.



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CLAIMS

[Claim(s)]

[Claim 1] The terminal formation approach of the wafer level CSP characterized by being based on the following process in the wafer level CSP completed by the individual fragmentation by the terminal formation and the dicing in wafer level.

b) while crushing said golden bump head by this copper foil by forming in the electrode on a semi-conductor wafer the golden bump by whom the head sharpened by wirebonding, and carrying out the laminating of the copper foil with RO resin to it -- a pressure welding -- carrying out -- Ha -- said copper foil on said golden bump -- an electrode -- etching -- forming -- NI -- give non-electrolyzed nickel plating and non-electrolyzed gilding to said formed electrode.

[Claim 2] The terminal formation approach of the wafer level CSP characterized by being based on the following process in the wafer level CSP completed by the individual fragmentation by the terminal formation and the dicing in wafer level.

b) Form the golden bump to whom the head sharpened by wirebonding in the electrode on a semi-conductor wafer. A pressure welding is carried out crushing said golden bump head by this copper foil by carrying out the laminating of the copper foil with RO resin. The golden bump head who overall etching removed [bump] the Ha aforementioned copper foil, and etchback of the surface resin was carried out [bump], and had said head crushed is exposed. Non-electrolytic copper plating and electrolytic copper plating are performed all over a NI front face, said golden bump head and connection are taken, an electrode is formed in said copper plating on the HO aforementioned golden bump by etching, and non-electrolyzed nickel plating and non-electrolyzed gilding are given to the electrode by which the HE aforementioned formation was carried out.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the manufacture approach of the semi-conductor wafer level CSP (chip-size package), and relates to the terminal formation approach.

[0002]

[Description of the Prior Art] While high-performance-izing of electronic equipment, advanced features, and a miniaturization progress, the wiring width of face in wafer level, wire-length shortening, high integration and wire-length shortening in package level, and a miniaturization are attained, and, as for semi-conductor components, improvement in the speed of semi-conductor components and a miniaturization are progressing quickly on the both sides of wafer level and package level. Invention of the various bump manufacture approaches aiming at connection with the electrode of a chip electrode, INTAPOZA, or a mounting substrate and the connection method by this bump and an improvement are contributing to evolution of semiconductor package level. The approach by wirebonding is widely learned by one of the bump manufacture approach of this. An example of the bump manufacture approach by the conventional wirebonding is shown in drawing 3. drawing 3 -- setting -- the capillary head 9 of a wire bonder to the gold streak 10 -- predetermined length -- sending -- this -- a gold streak -- ten head -- the discharge from a torch 11 -- spherical -- rounding off -- after that -- a capillary -- descending -- said gold streak -- 10 head spherical section is contacted to an electrode 12, and it joins to an electrode 12 by heating and supersonic vibration. A gold streak 10 is torn off by fixing a gold streak 10 by the clumper 13, pulling up a capillary, and the golden bump 14 by whom the head sharpened is formed. Although omitted by a diagram, the golden bump 14 by whom the head formed above usually sharpened makes a top face flat with a leveling tool, and performs leveling which arranges two or more golden bumps' height formed similarly.

[0003]

[Problem(s) to be Solved by the Invention] However, the conventional bump manufacture approach shown in drawing 3 has that dispersion arises to the die length of the head configuration when tearing off a gold streak, and the fault that distortion arises in a bump configuration when leveling the sharp head. Moreover, as for the golden bump who finished leveling, it is common not to make it a package electrode as it is, but to connect with a package electrode through INTAPOZA etc. This invention was made in order to solve the above-mentioned technical problem, is carried out as it is, and is used, without leveling the golden bump at the sharp head which the above tore off and was made, and this bump is further provided with the approach of forming the terminal of the wafer level CSP by forming a direct package electrode.

[0004]

[Means for Solving the Problem] The terminal formation approach of the wafer level CSP of claim 1 is characterized by being based on the following process in the wafer level CSP completed by the individual fragmentation by the terminal formation and the dicing in wafer level.

b) while crushing said golden bump head by this copper foil by forming in the electrode on a

semi-conductor wafer the golden bump by whom the head sharpened by wirebonding, and carrying out the laminating of the copper foil with RO resin to it -- a pressure welding -- carrying out -- Ha -- said copper foil on said golden bump -- an electrode -- etching -- forming -- NI -- give non-electrolyzed nickel plating and non-electrolyzed gilding to said formed electrode.

[0005] According to the terminal formation approach of the wafer level CSP of claim 1, two or more golden bumps are formed in uniform height by that of copper foil push **** in the golden bump by whom the head sharpened, and the pressure welding of the copper foil and the golden bump who become an electrode is carried out certainly simultaneously. Moreover, since an electrode is formed by etching, two or more electrode alignment precision of its is stable from a 2 steps of bumps pile method.

[0006] The terminal formation approach of the wafer level CSP of claim 2 is characterized by being based on the following process in the wafer level CSP completed by the individual fragmentation by the terminal formation and the dicing in wafer level.

b) Form the golden bump to whom the head sharpened by wirebonding in the electrode on a semi-conductor wafer. A pressure welding is carried out crushing said golden bump head by this copper foil by carrying out the laminating of the copper foil with RO resin. The golden bump head who overall etching removed [bump] the Ha aforementioned copper foil, and etchback of the surface resin was carried out [bump], and had said head crushed is exposed. Non-electrolytic copper plating and electrolytic copper plating are performed all over a NI front face, said golden bump head and connection are taken, an electrode is formed in said copper plating on the HO aforementioned golden bump by etching, and non-electrolyzed nickel plating and non-electrolyzed gilding are given to the electrode by which the HE aforementioned formation was carried out.

[0007] According to the terminal formation approach of the wafer level CSP of claim 2, two or more golden bumps are formed in uniform height by that of copper foil push **** in the golden bump by whom the head sharpened. Moreover, since the golden bump head who etchback of the surface resin was carried out [bump] and had said head crushed is exposed, plating connection of copper plating and the golden bump who become an electrode is made in a large area. Moreover, since an electrode is formed by etching, two or more electrode alignment precision of its is stable from a 2 steps of bumps pile method.

[0008]

[Embodiment of the Invention] This invention is explained to a detail based on a drawing. Drawing 1 shows the CSP electrode formation process which is 1 operation gestalt of this invention by the side-face mimetic diagram. Drawing 1 (a) shows the condition of having formed the golden bump 3 by whom the head sharpened by the conventional approach using the wire bonder on the aluminum electrode of semi-conductor wafer 1 front face, or the copper electrode 2. Drawing 1 (b) is a thing in the condition of having carried out heating application of pressure and having carried out the laminating of the copper foil with resin (what applied epoxy semi-hardening resin to copper foil) to the thing of said condition. Copper foil thickness sets to about 75 micrometers, resin thickness is set to 50-60 micrometers, the point in which the golden bump 3 sharpened is crushed by copper foil 5, and it is made to fix with an epoxy resin 4, where copper foil 5 is electrically connected by the pressure welding with the golden bump 3. Here, the copper foil thickness and resin thickness to be used shall be suitably changed from the above-mentioned value, a bump's magnitude, i.e., electrode pitch, and shall select an optimum value.

[0009] Next, a resist film is stuck on copper foil 5 front face, and as the mask film of an electrode pattern is exposed, developed and etched in piles and it is shown in drawing 1 (c), a copper electrode 6 is formed. Non-electrolyzed nickel plating and non-electrolyzed gilding 7 are given to the above-mentioned copper electrode 6, and it is made to complete as an electrode, as shown in drawing 1 (d). Then, although omitted by a diagram, cutting separation is carried out by dicing at each IC, and the wafer level CSP is completed.

[0010] Drawing 2 explains how to form an electrode by carrying out copper plating of a golden bump and the copper foil to a golden bump to the approach of making pressure-welding connection as mentioned above. Since (a) of drawing 2 and (b) take the same process as drawing

1 (a) and (b), they omit explanation. As shown in drawing 2 (c), etching removes after [a laminating] copper foil altogether, and as shown in drawing 2 (d), etchback which roughens some epoxy resins and is etched is performed. The chemical approach of using permanganic acid etc. is easy for etchback. Since the golden bump head where the head collapsed projects from resin and it exposes with this etchback as drawing 2 (d) shows, connection area with copper plating performed later can be increased. Drawing 2 (d) shows the condition of having attached about 75-micrometer copper with the electrolytic copper plating 8 after non-electrolytic copper plating. Here, it is desirable that the direction which reduces the thickness of copper plating with an electrode pitch selects an optimum value with a chip size since the result configuration of an electrode becomes good.

[0011] Like the process of drawing 1 (c) and (d), after said copper plating forms an electrode through resist film pasting, electrode pattern exposure, development, etching, non-electrolyzed nickel plating, and non-electrolyzed gilding, finally carries out cutting separation by dicing at each IC, and completes the wafer level CSP.

[0012]

[Effect of the Invention] Since the golden bump who formed in the electrode on a wafer becomes the stress relief to the heat stress after mounting CSP to a substrate according to this invention, a longevity life with high connection dependability is guaranteed.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] A side-face mimetic diagram shows the CSP electrode formation process which is 1 operation gestalt of this invention.

[Drawing 2] A side-face mimetic diagram shows the CSP electrode formation process which is the second example of this invention.

[Drawing 3] A side-face mimetic diagram shows the example of the bump manufacture approach by the conventional wirebonding.

[Description of Notations]

1 Semi-conductor Wafer

2 Aluminum Electrode or Copper Electrode

3 Golden Bump

4 Epoxy Resin

5 Copper Foil

6 Copper Electrode

7 Non-Electrolyzed Nickel Plating and Non-Electrolyzed Gilding

8 After [Non-Electrolytic Copper Plating] Electrolytic Copper Plating

9 Capillary Head

10 Gold Streak

11 Torch

12 Electrode

13 Clamper

14 Golden Bump

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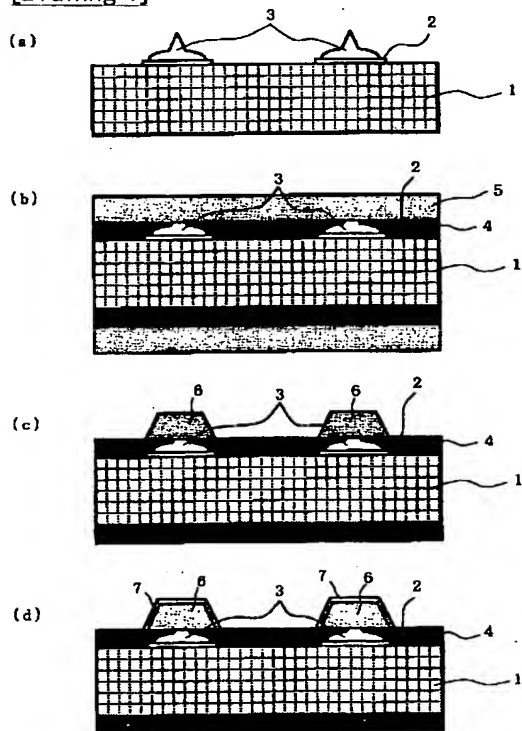
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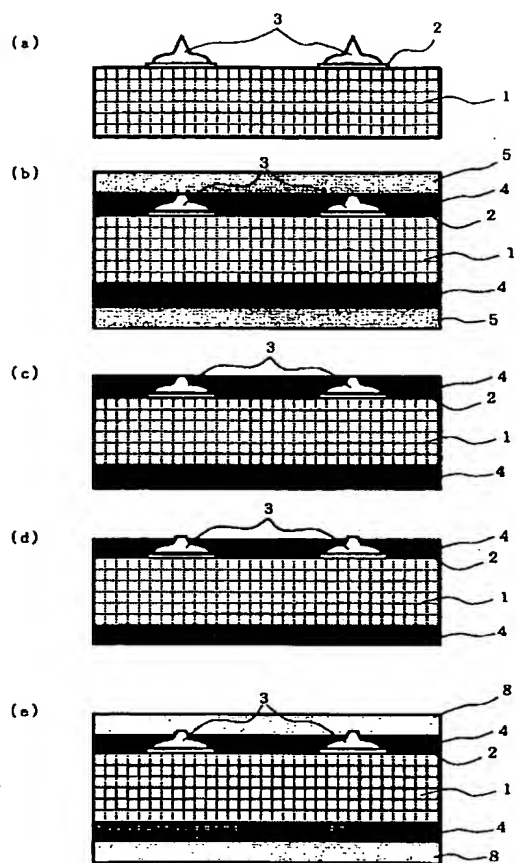
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DRAWINGS

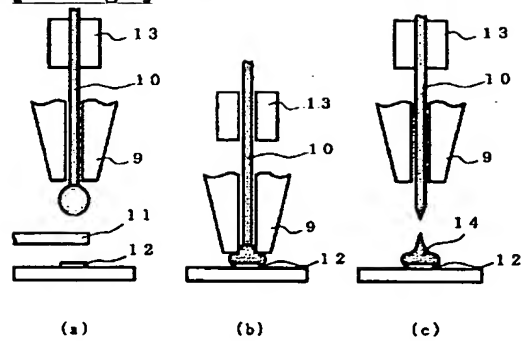
[Drawing 1]



[Drawing 2]



[Drawing 3]



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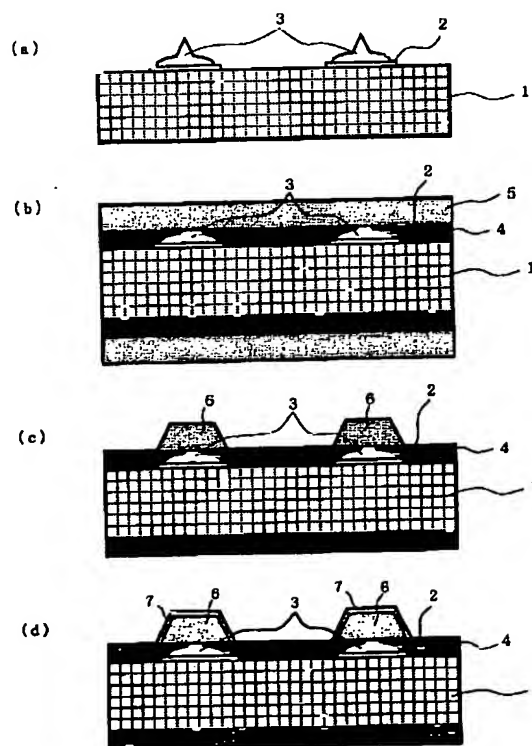
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(54)【発明の名称】 ウェハレベルCSPの端子形成方法

(57)【要約】

【課題】ワイヤボンディング法により形成した尖った先端の金バンパをレベリングせずにそのまま使用し、さらに、該バンパに直接パッケージ電極を形成することでウェハレベルCSPの端子を形成する方法を提供する。

【解決手段】半導体ウェハ表面のアルミ電極または銅電極上にワイヤボンダを使用した従来方法により先端の尖った金バンパを形成し、樹脂付き銅箔を加熱加圧して積層する。ここで、銅箔厚は約75 μ m、樹脂厚はバンパの大きさにもよるが50~60 μ mとし、金バンパの尖った先端部が銅箔で押し潰され、金バンパと銅箔が圧接により電氣的に接続された状態でエポキシ樹脂により固着されるようにする。次いで、銅箔をエッチングすることにより電極を形成する。



【特許請求の範囲】

【請求項1】 ウェハレベルでの端子形成とダイシングによる個体分断で完成するウェハレベルCSPにおいて、次の工程によることを特徴とするウェハレベルCSPの端子形成方法。

イ) 半導体ウェハ上の電極にワイヤボンディングで先端の尖った金バンパを形成し、ロ) 樹脂付き銅箔を積層することで該銅箔により前記金バンパ先端を押し潰しながら圧接し、ハ) 前記金バンパ上の前記銅箔に電極をエッチングで形成し、ニ) 前記形成された電極に無電解ニッケルめっきと無電解金めっきを施す。

【請求項2】 ウェハレベルでの端子形成とダイシングによる個体分断で完成するウェハレベルCSPにおいて、次の工程によることを特徴とするウェハレベルCSPの端子形成方法。

イ) 半導体ウェハ上の電極にワイヤボンディングで先端の尖った金バンパを形成し、ロ) 樹脂付き銅箔を積層することで該銅箔により前記金バンパ先端を押し潰しながら圧接し、ハ) 前記銅箔を全面エッチングにより除去し、表面樹脂をエッチバックして前記先端を押し潰された金バンパ頭部を露出させ、ニ) 表面全面に無電解銅めっきおよび電解銅めっきを施し前記金バンパ頭部と接続をとり、ホ) 前記金バンパ上の前記銅めっきに電極をエッチングで形成し、ヘ) 前記形成された電極に無電解ニッケルめっきと無電解金めっきを施す。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は半導体ウェハレベルCSP（チップサイズパッケージ）の製造方法に係り、端子形成方法に関するものである。

【0002】

【従来の技術】電子機器の高性能化、高機能化、小型化が進むなかで、半導体部品はウェハレベルでの配線幅、配線長短縮化と高集積化、パッケージレベルでの配線長短縮化と小型化が図られ、ウェハレベルとパッケージレベルの双方で急速に半導体部品の高速化、小型化が進んでいる。半導体パッケージレベルの進化には、チップ電極とインタポーザまたは実装基板の電極との接続を目的とした各種バンパ製造方法および該バンパによる接続方法の発明、改善が貢献している。このバンパ製造方法の一つにワイヤボンディングによる方法が広く知られている。従来のワイヤボンディングによるバンパ製造方法の一例を図3に示す。図3において、ワイヤボンダのキャピラリ先端9から金線10を所定長だけ出し、該金線10先端をトーチ11からの放電で球状に丸め、その後キャピラリを下降して前記金線10先端球状部を電極12に接触させ、加熱と超音波振動により電極12に接合する。キャピラリを引き上げながら金線10をクランプ13で固定することで金線10を引きちぎり、先端が尖った金バンパ14が形成される。図では省略するが、通

常、前記で形成された先端が尖った金バンパ14は、レベリングツールによって上面を平坦にし、同様に形成した複数の金バンパの高さを揃えるレベリングを行なう。

【0003】

【発明が解決しようとする課題】しかしながら、図3に示した従来のバンパ製造方法は、金線を引きちぎった時の先端形状の長さにばらつきが生じることと、尖った先端をレベリングする時にバンパ形状に歪みが生ずるという欠点がある。また、レベリングを終えた金バンパはそのままパッケージ電極にせず、インタポーザ等を介してパッケージ電極に接続されるのが一般的である。本発明は、上記課題を解決するためになされたもので、前記の引きちぎってできた尖った先端の金バンパをレベリングせずにそのまま使用し、さらに、該バンパに直接パッケージ電極を形成することでウェハレベルCSPの端子を形成する方法を提供する。

【0004】

【課題を解決するための手段】請求項1のウェハレベルCSPの端子形成方法は、ウェハレベルでの端子形成とダイシングによる個体分断で完成するウェハレベルCSPにおいて、次の工程によることを特徴とする。

イ) 半導体ウェハ上の電極にワイヤボンディングで先端の尖った金バンパを形成し、ロ) 樹脂付き銅箔を積層することで該銅箔により前記金バンパ先端を押し潰しながら圧接し、ハ) 前記金バンパ上の前記銅箔に電極をエッチングで形成し、ニ) 前記形成された電極に無電解ニッケルめっきと無電解金めっきを施す。

【0005】請求項1のウェハレベルCSPの端子形成方法によれば、先端の尖った金バンパを銅箔押し潰すので、複数の金バンパは均一な高さに形成され、同時に、電極となる銅箔と金バンパは確実に圧接される。また、電極はエッチングにより形成するので、複数の電極整列精度がバンパ二段重ね方式よりも安定する。

【0006】請求項2のウェハレベルCSPの端子形成方法は、ウェハレベルでの端子形成とダイシングによる個体分断で完成するウェハレベルCSPにおいて、次の工程によることを特徴とする。

イ) 半導体ウェハ上の電極にワイヤボンディングで先端の尖った金バンパを形成し、ロ) 樹脂付き銅箔を積層することで該銅箔により前記金バンパ先端を押し潰しながら圧接し、ハ) 前記銅箔を全面エッチングにより除去し、表面樹脂をエッチバックして前記先端を押し潰された金バンパ頭部を露出させ、ニ) 表面全面に無電解銅めっきおよび電解銅めっきを施し前記金バンパ頭部と接続をとり、ホ) 前記金バンパ上の前記銅めっきに電極をエッチングで形成し、ヘ) 前記形成された電極に無電解ニッケルめっきと無電解金めっきを施す。

【0007】請求項2のウェハレベルCSPの端子形成方法によれば、先端の尖った金バンパを銅箔押し潰すので、複数の金バンパは均一な高さに形成される。また、

表面樹脂をエッチバックして前記先端を押し潰された金バンプ頭部を露出させるので、電極となる銅めっきと金バンプは広い面積でめっき接続される。また、電極はエッチングにより形成するので、複数の電極整列精度がバンプ二段重ね方式よりも安定する。

【0008】

【発明の実施の形態】図面を基に本発明を詳細に説明する。図1は本発明の一実施形態であるCSP電極形成工程を側面模式図で示す。図1(a)は、半導体ウェハ1表面のアルミ電極または銅電極2上に、ワイヤボンダを使用して従来方法により先端の尖った金バンプ3を形成した状態を示す。図1(b)は、前記状態のものに、樹脂付き銅箔(銅箔にエポキシ半硬化樹脂を塗布したもの)を加熱加圧して積層した状態のものである。銅箔厚は約75 μ m、樹脂厚は50~60 μ mとし、金バンプ3の尖った先端部が銅箔5で押し潰され、金バンプ3と銅箔5が圧接により電氣的に接続された状態でエポキシ樹脂4により固着されるようにする。ここで、使用する銅箔厚と樹脂厚は、バンプの大きさすなわち電極ピッチにより上記値から適宜変更して最適値を選定するものとする。

【0009】次に銅箔5表面にレジストフィルムを貼付し、電極パターン用のマスクフィルムを重ねて露光、現像、エッチングして図1(c)に示すように銅電極6を形成する。上記銅電極6に無電解ニッケルめっきおよび無電解金めっき7を施し、図1(d)に示すように電極として完成させる。その後、図では省略するが、ダイシングにより個々のICに切断分離してウェハレベルCSPを完成する。

【0010】上記のように金バンプと銅箔を圧接接続する方法に対し、金バンプに銅めっきすることで電極を形成する方法を図2で説明する。図2の(a)と(b)は、図1(a)、(b)と同じ工程を採るので説明を省略する。図2(c)に示すように、積層後銅箔をエッチングにより全て除去し、図2(d)に示すように、エポキシ樹脂の一部を粗化、エッチングするエッチバックを行なう。エッチバックには過マンガン酸などを用いる化学的方法が容易である。該エッチバックにより、図2(d)で示すように、先端が潰れた金バンプ頭部が樹脂から突起して露出するので、後で行なう銅めっきとの接

続面積を増加することができる。図2(d)は、無電解銅めっき後電解銅めっき8により約75 μ mの銅を付けた状態を示す。ここで、電極ピッチにより銅めっきの厚みを減らす方が電極の仕上がり形状が良好になるので、チップサイズによって最適値を選定することが好ましい。

【0011】前記銅めっき後は、図1(c)、(d)の工程と同様に、レジストフィルム貼付、電極パターン露光、現像、エッチング、無電解ニッケルめっき、無電解金めっきを経て電極を形成し、最後にダイシングにより個々のICに切断分離してウェハレベルCSPを完成する。

【0012】

【発明の効果】本発明によれば、ウェハ上の電極に形成した金バンプが、CSPを基板へ実装した後の熱ストレスに対するストレスリリーフとなるので、接続信頼性の高い長寿命が保証される。

【図面の簡単な説明】

【図1】本発明の一実施形態であるCSP電極形成工程を側面模式図で示す。

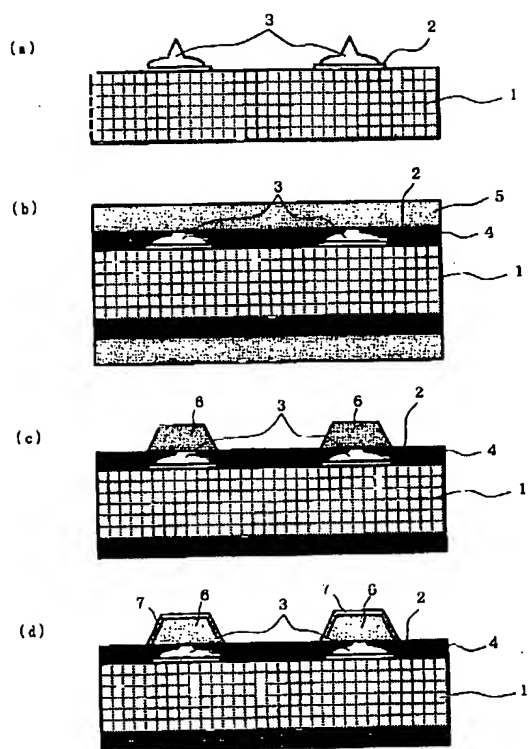
【図2】本発明の二番目の実施例であるCSP電極形成工程を側面模式図で示す。

【図3】従来のワイヤボンディングによるバンプ製造方法の例を側面模式図で示す。

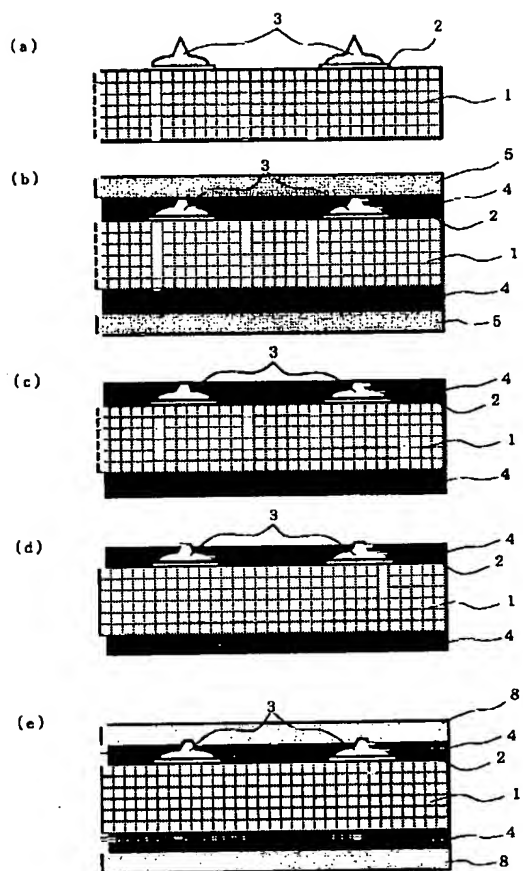
【符号の説明】

- 1 半導体ウェハ
- 2 アルミ電極または銅電極
- 3 金バンプ
- 4 エポキシ樹脂
- 5 銅箔
- 6 銅電極
- 7 無電解ニッケルめっきおよび無電解金めっき
- 8 無電解銅めっき後電解銅めっき
- 9 キャピラリ先端
- 10 金線
- 11 トーチ
- 12 電極
- 13 クランパ
- 14 金バンプ

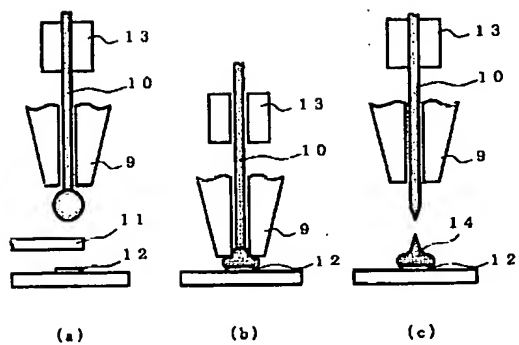
【図1】



【図2】



【図3】



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